



# A Priori Wire Length Estimates for Digital Design

*Dirk Stroobandt*

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## **A Priori Wire Length Estimates for Digital Design** Dirk Stroobandt

The roots of this book, and of the new research field that it defines, lie in the scaling of VLSI technology. With gigahertz system clocks and ever accelerating design and process innovations, interconnects have become the limiting factor for both performance and density. This increasing impact of interconnects on the system implementation space necessitates new tools and analytic techniques to support the system designer. With respect to modeling and analysis, the response to interconnect dominance is evolutionary. Atomistic- and grain-level models of interconnect structure, and performance models at multi-gigahertz operating frequencies, together guide the selection of improved materials and process technologies (e. g. , damascene copper wires, low-permittivity dielectrics). Previously in significant effects (e. g. , mutual inductance) are added into performance models, as older approximations (e. g. , lumped-capacitance gate load models) are discarded. However, at the system-level and chip planning level, the necessary response to interconnect dominance is revolutionary. Convergent design flows do not require only distributed RLC line models, repeater awareness, unifications with extraction and analysis, etc. Rather, issues such as wiring layer assignment, and early prediction of the resource and performance envelope for the system interconnect (in particular, based on statistical models of the system interconnect structure), also become critical. Indeed, system-level interconnect prediction has emerged as the enabler of improved interconnect modeling, more cost-effective system architectures, and more productive design technology.

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